AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A card with a microprocessor and ~~contacts~~ at least one contact, and a communication device in the form of a hard-wired circuit disposed between the ~~contacts~~ contact and the microprocessor that checks the integrity of signals transmitted between the microprocessor and a terminal, wherein said communication device includes:

means to determine whether an item of information received by the card from the terminal is erroneous; and

means to generate and return at least one item of information to the terminal which is a function of ~~the signals received from the terminal~~ said determination.

2. (Currently Amended) A card with a microprocessor and ~~contacts~~ at least one contact according to Claim 1, wherein the communication device comprises:

- a circuit for analysing electrical signals transmitted by the terminal so as to supply a series of electrical pulses,

- a circuit for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code indicating the status of the check,

- a circuit for determining each character from the pulses in the series,

- a first plurality of registers for recording characters of a command and an address supplied by the character determination circuit and making them available to the microprocessor,

- a second plurality of registers for recording characters of data supplied by the character determination circuit and making them available to the microprocessor,

- a circuit for acknowledging the command, associated with the first plurality of registers, for analysing the characters of the command and supplying a code indicating a command reception status,

- a third plurality of registers for recording codes for the data and for the status of execution of the command supplied by the microprocessor, and

- a circuit for transmitting to the terminal the codes supplied by the checking circuit, the command acknowledgement circuit and the third plurality of registers.

3. (Currently Amended) A card with microprocessor and ~~contacts~~ at least one contact according to Claim 2, wherein the analysis circuit detects the signals transmitted and presents them in the form of a series of binary electrical pulses.

4. (Currently Amended) A card with a microprocessor and ~~contacts~~ at least one contact according to Claim 2 wherein the checking circuit checks for a binary parity digit or a cyclic redundancy code and supplies a corresponding signal or code.

5. (Currently Amended) A card with a microprocessor and ~~contacts~~ at least one contact card according to Claim 3, wherein the checking circuit checks for

a binary parity digit or a cyclic redundancy code and supplies a corresponding signal or code.

6. (Previously Presented) The card of claim 1, wherein the item of information generated by said generating means comprises an indication whether a signal received from the terminal contains an error.

7. (Previously Presented) The card of claim 6, wherein said generating means generates said indication on the basis of redundant information contained in the received signal.

8. (Previously Presented) The card of claim 1, wherein the item of information generated by said generating means comprises an indication whether a command contained in a signal received from the terminal is complete and correct.

9. (Previously Presented) The card of claim 1, wherein said communication device operates according to an asynchronous communication protocol.

Specifically, claim 1 recites that the communication device includes means to determine whether an item of information received by the card, from the terminal, is erroneous, and means to generate and return at least one item of information to the terminal which is a function of this determination. The Yamaguchi patent does not disclose that the UART 7a is capable of making such a determination. The structure of the UART is illustrated in Figure 2 of the Yamaguchi patent. As can be seen, it comprises a shift register 71, a pair of input and output buffers 72 and 73, and a flip-flop 75. These circuits do not detect whether an item of information received from the terminal is erroneous and generate a signal that is returned to the terminal which is a function of such a determination. Rather, the general objective of the Yamaguchi patent is to preserve battery power, by limiting the times during which a clock signal is output externally of the card (col. 2, line 66 to col. 3, line 5). Within this context, the function of the UART is to detect the start bit at the beginning of a data transmission (col. 8, lines 61-63). In the absence of a start bit, the external clock signal is inhibited.

Thus, the Yamaguchi patent does not disclose that the UART is capable of detecting whether information received from the terminal is erroneous, e.g. by checking parity, and generating a signal that is returned to the terminal to indicate this fact. It is noted that, at col. 9, lines 14-31, the Yamaguchi patent refers to a UART having a byte resending function, as disclosed in U.S. Patent No. 4,556,958. Again, however, this patent does not disclose a UART that performs the functions of the communication device recited in claim 1. In particular, the '958 patent does not disclose that a parity check is performed in the UART (port circuit 7). Rather, it is carried out by the microprocessor. In particular, the operations described at col. 7,